

Fig. 1

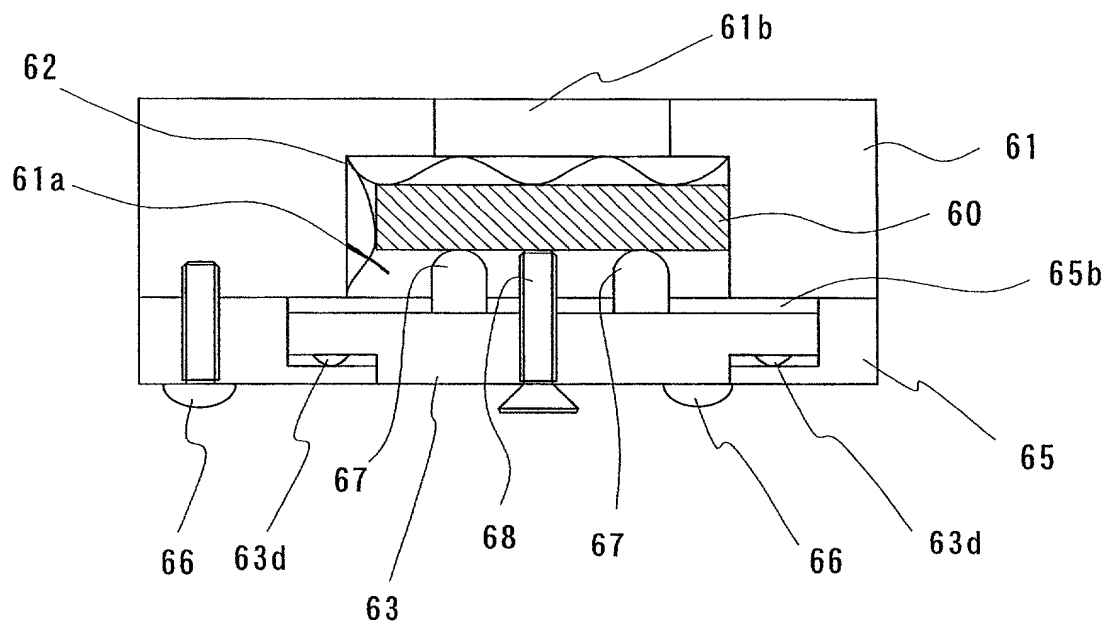


Fig. 2

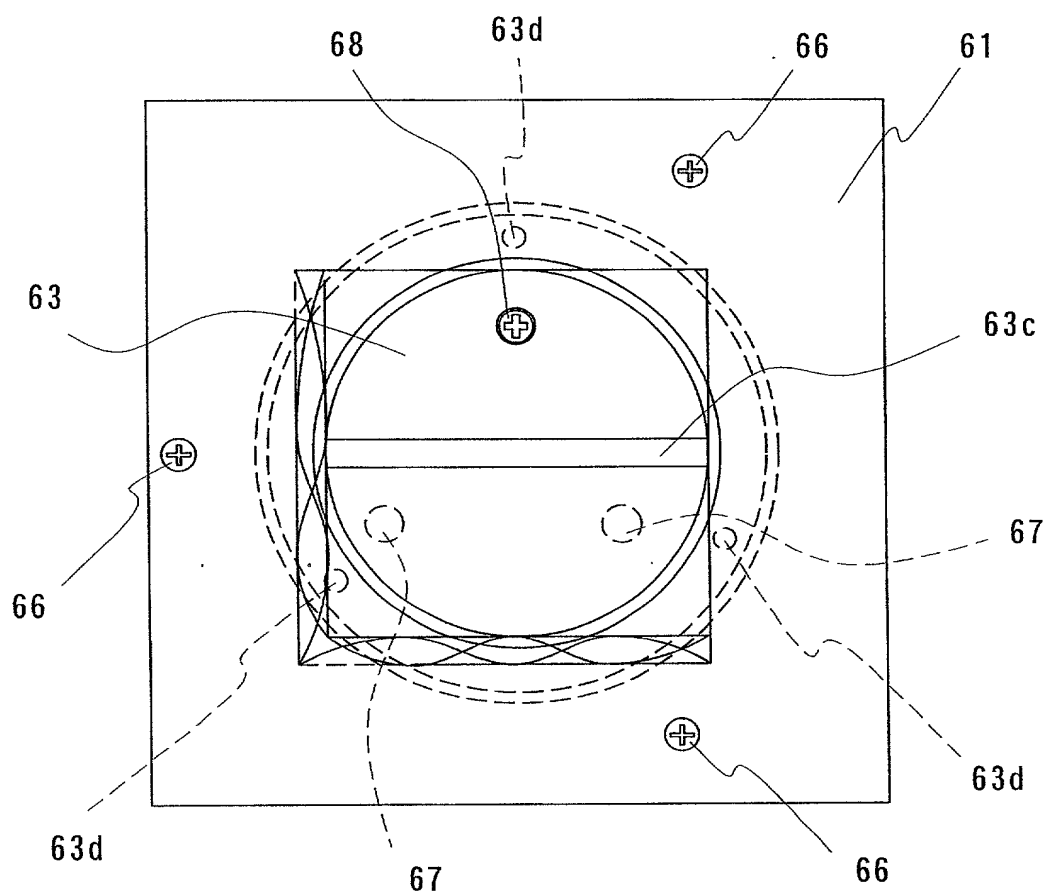


Fig. 3

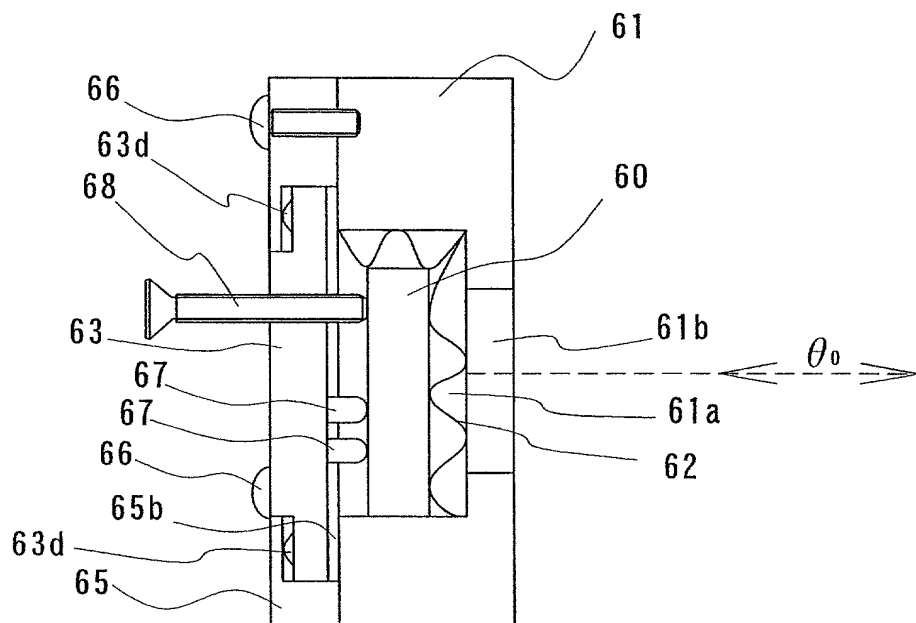


Fig. 4

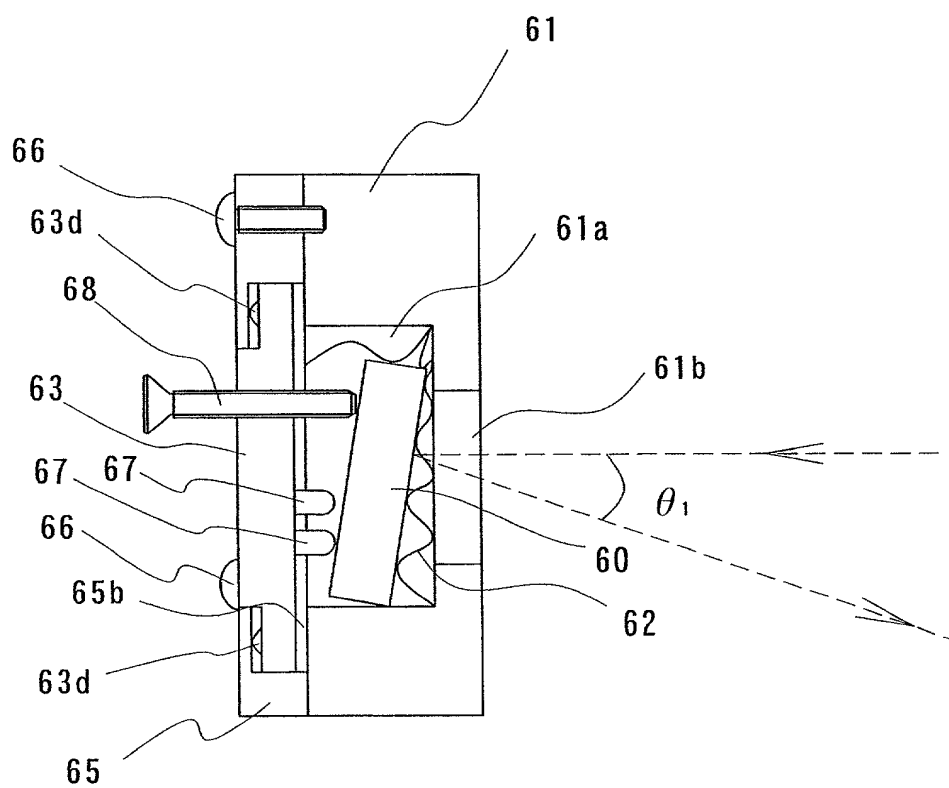


Fig. 5

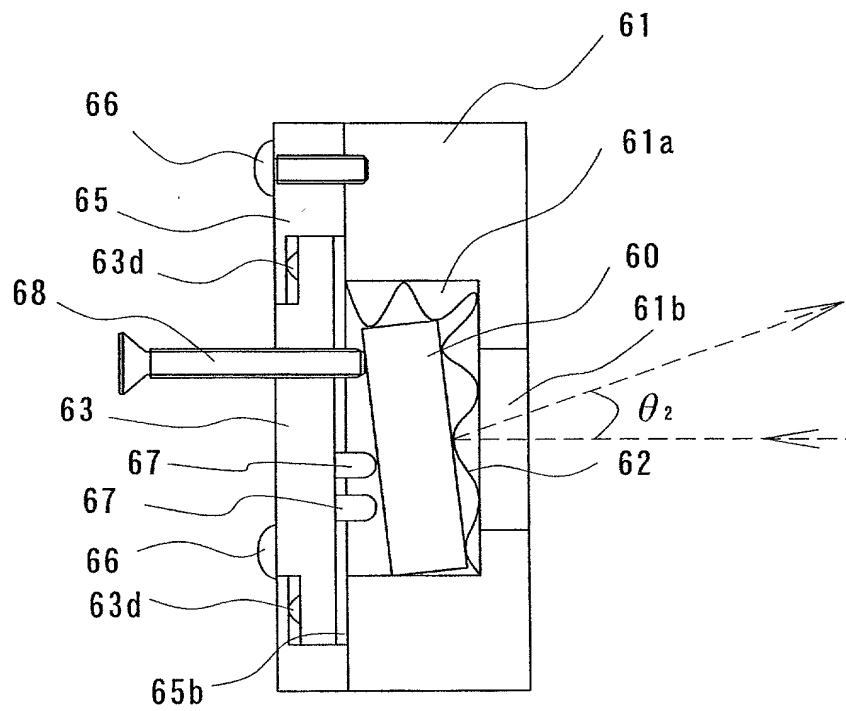


Fig. 6

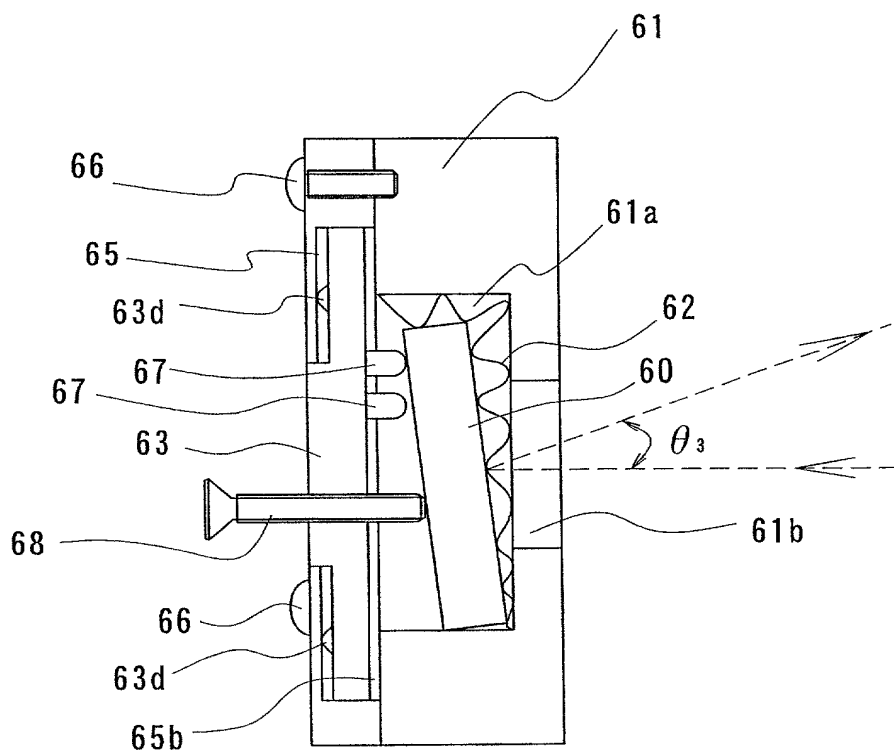


Fig. 7

Fig. 6 is a cross-sectional view of a semiconductor device. The device includes a substrate 61 with a central layer 60. A gate structure 62 is formed on top of layer 60. Below layer 60, there are two vertical structures 63 and 63d, and two horizontal structures 66 and 66d. A central vertical structure 68 is also shown. The device is surrounded by a frame 65.

Fig. 9

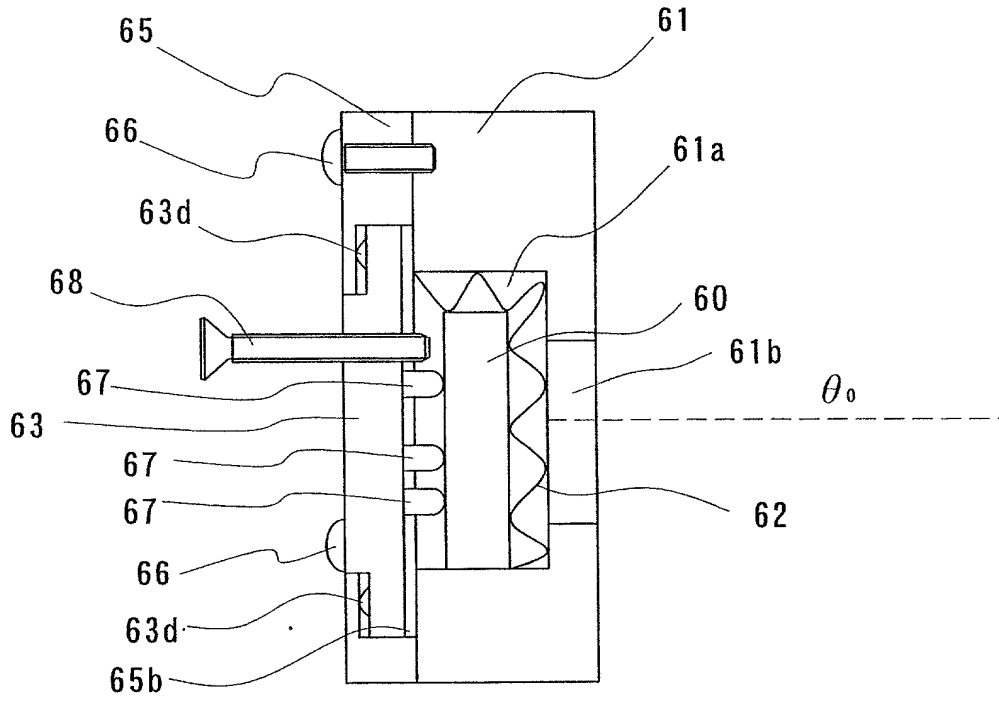


Fig. 10

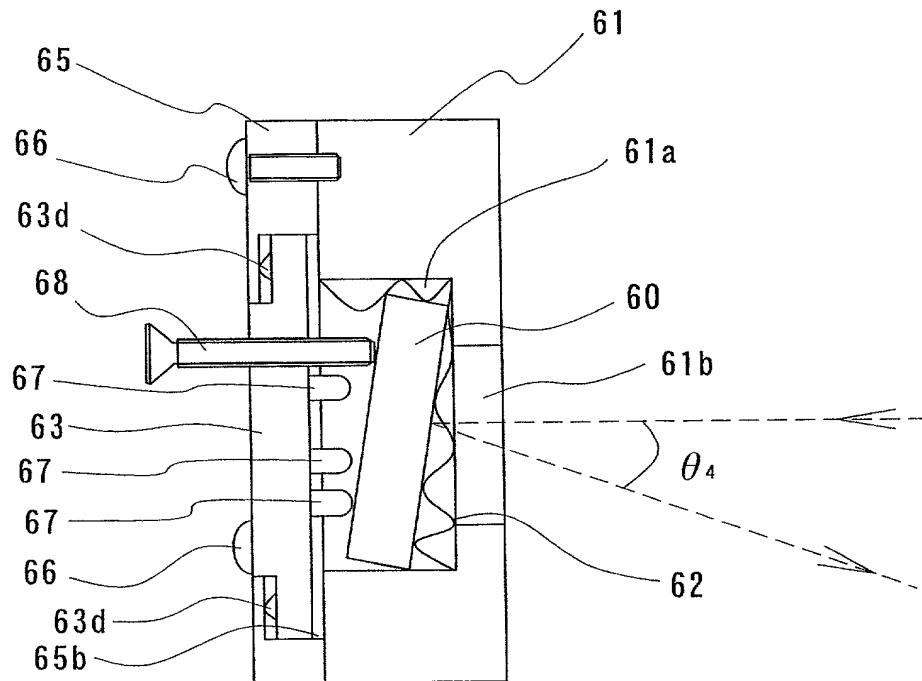


Fig. 11

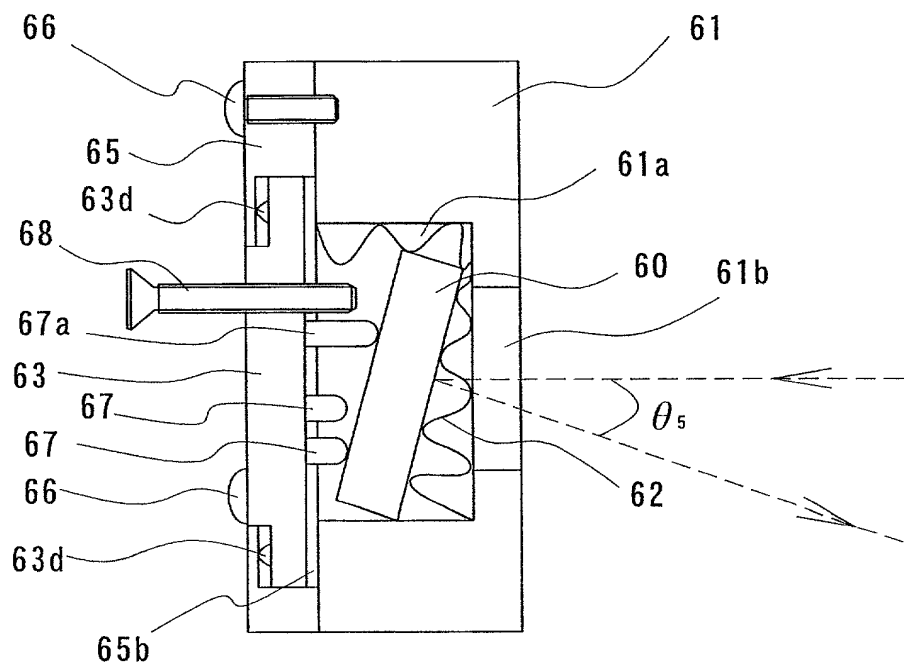


Fig. 12

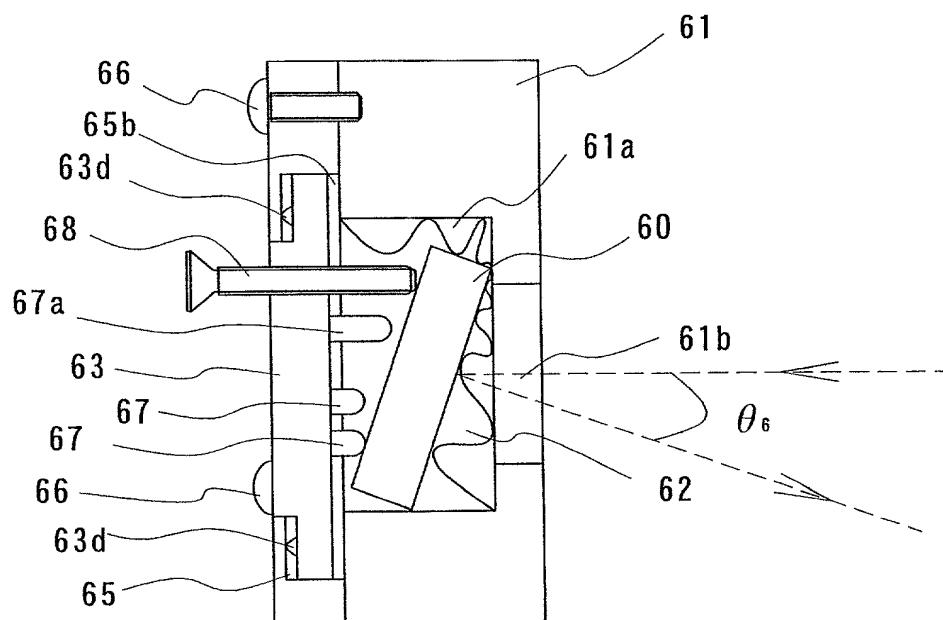


Fig. 13

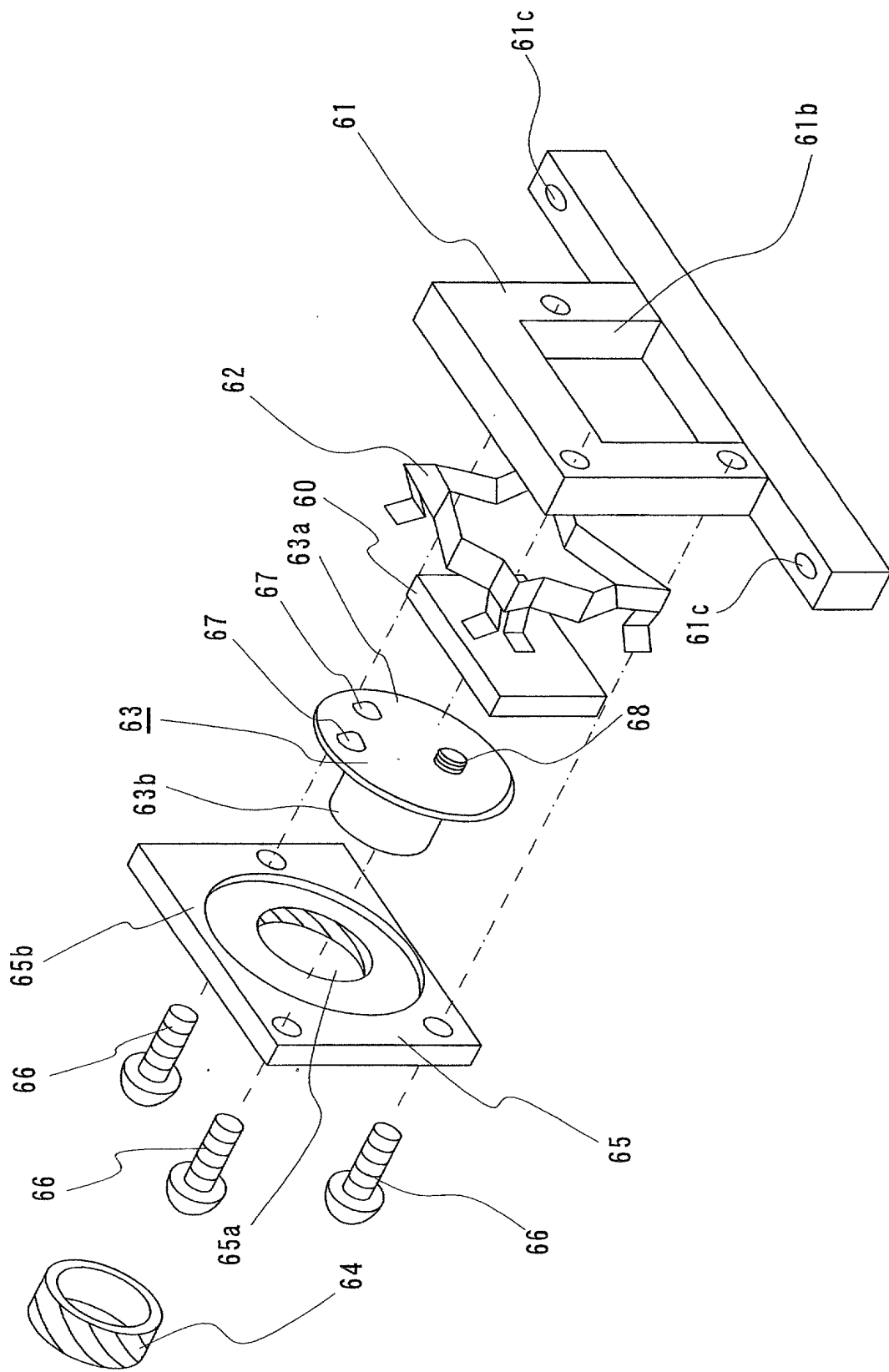


Fig. 14



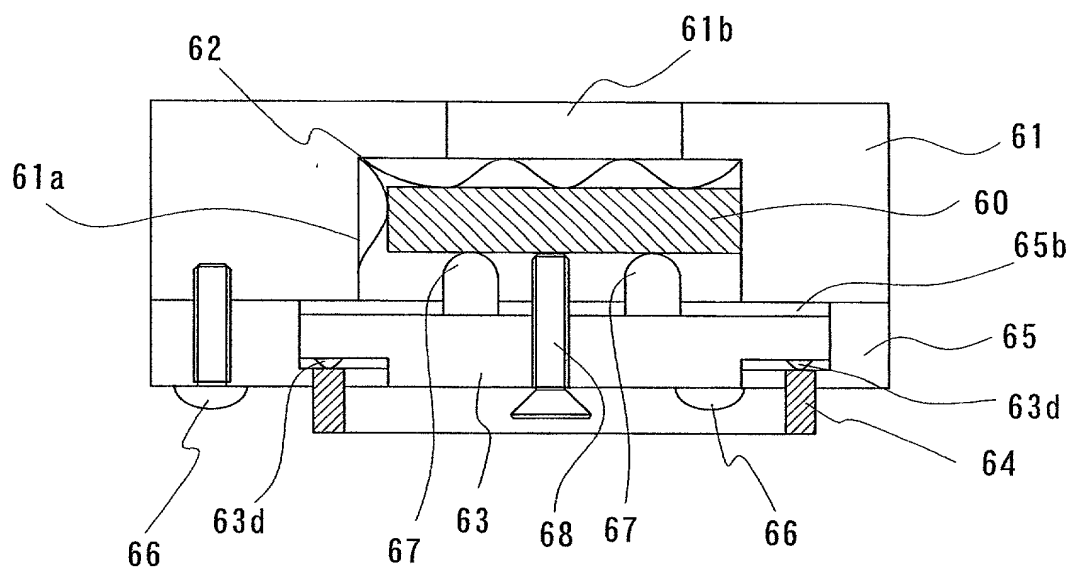


Fig. 15

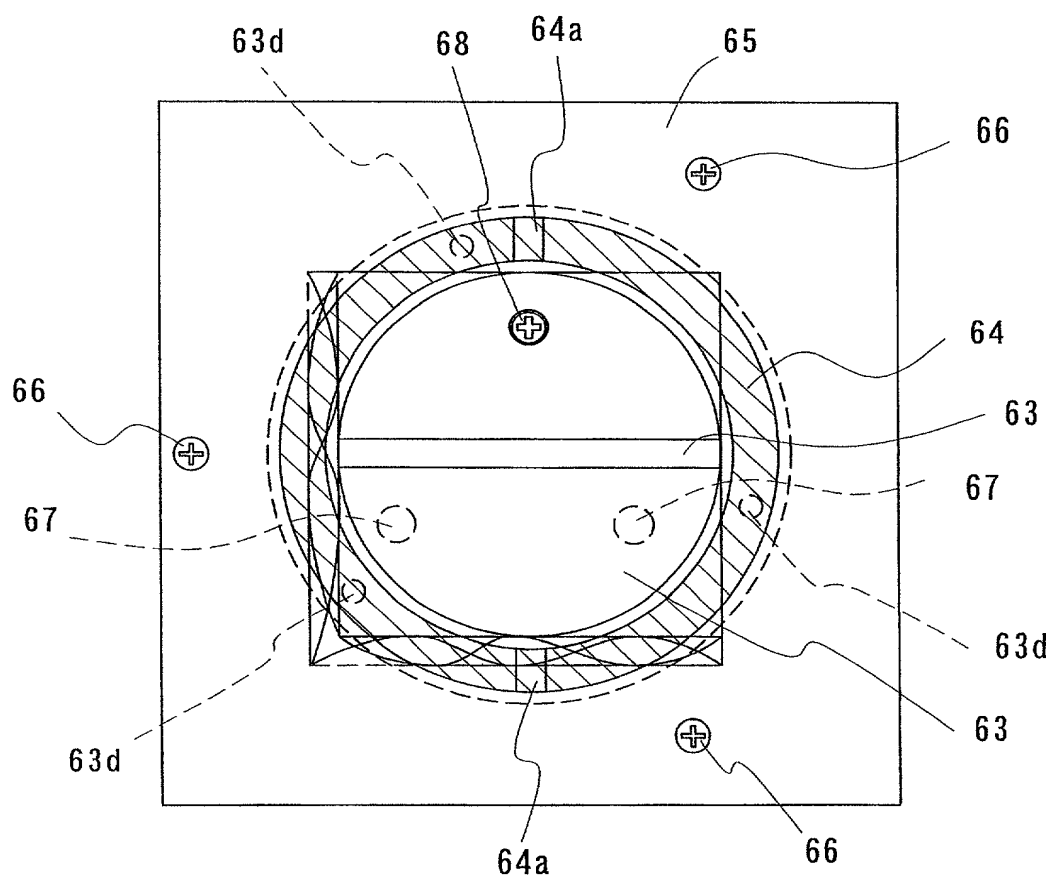


Fig. 16

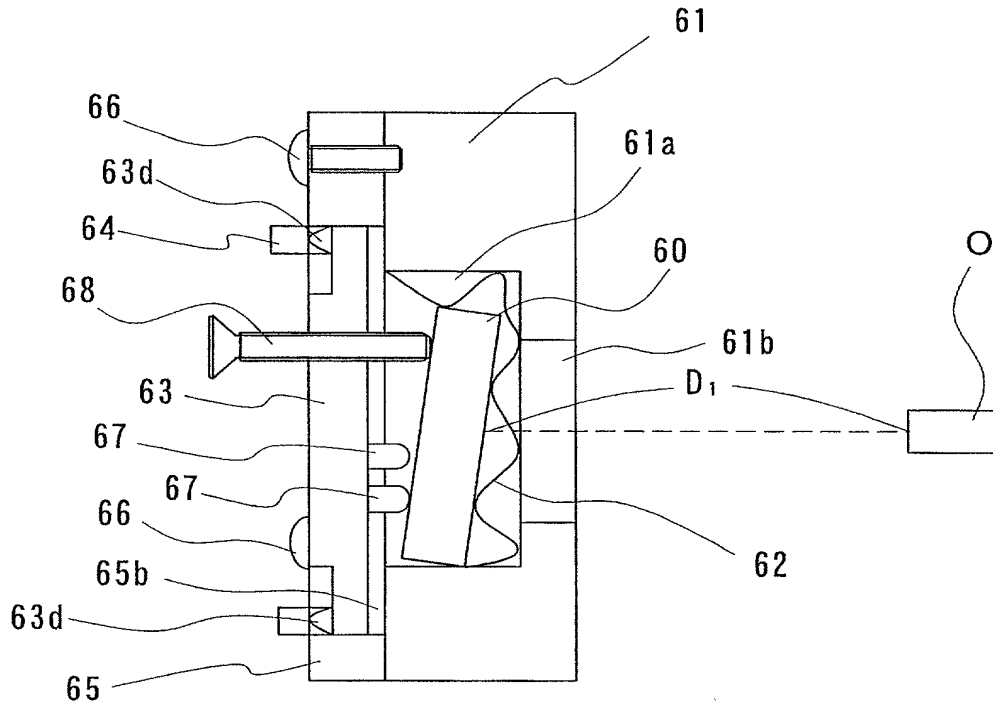


Fig. 17

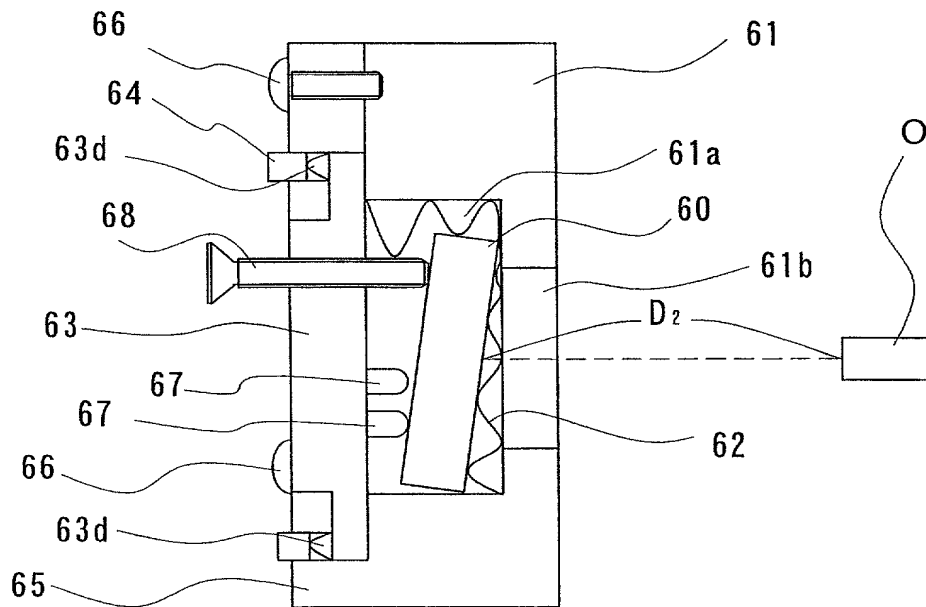


Fig. 18

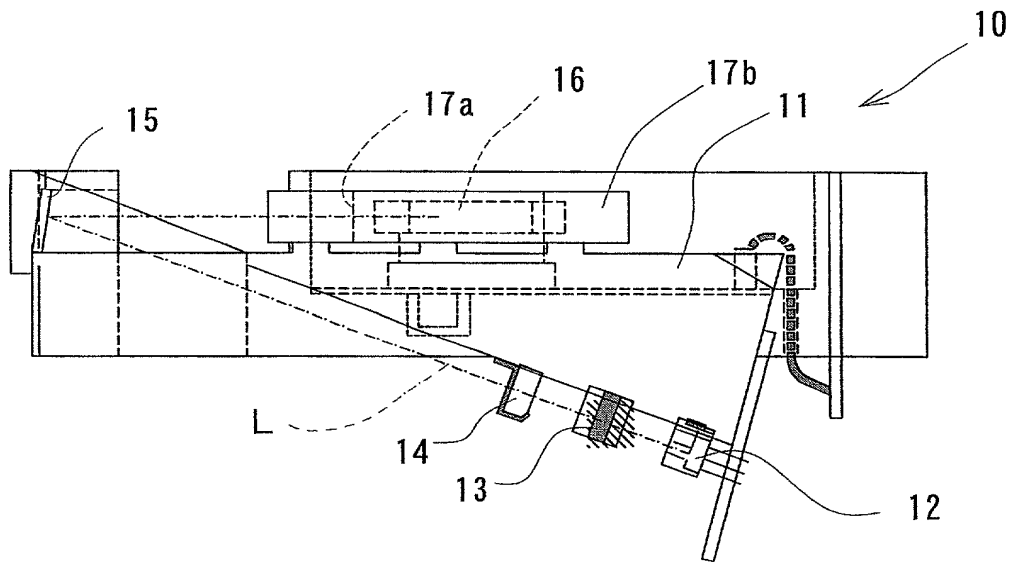


Fig. 19

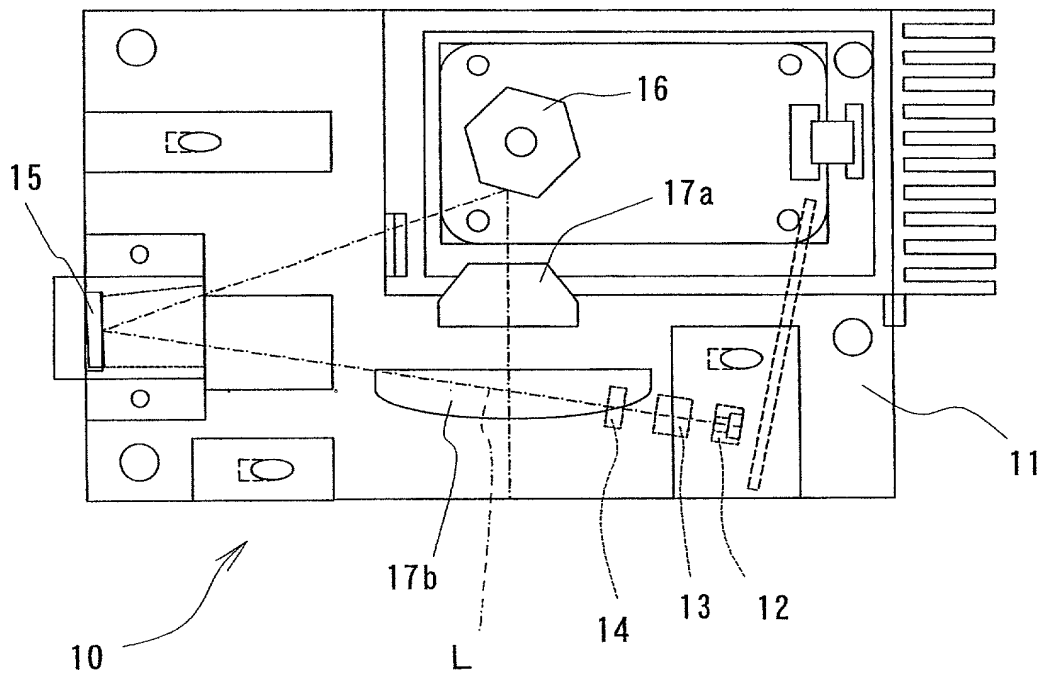


Fig. 20

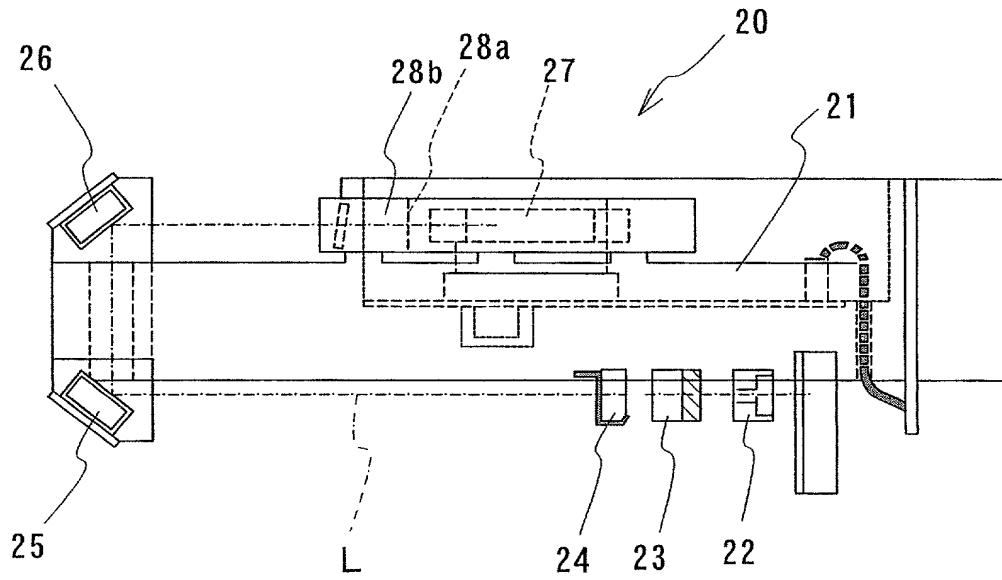


Fig. 21

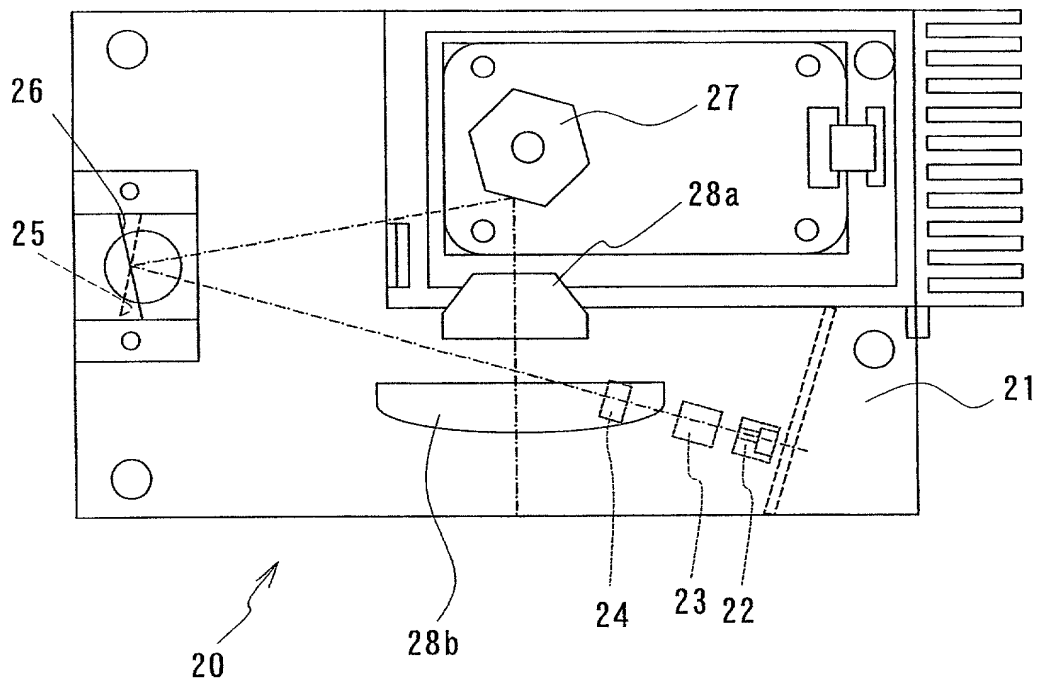


Fig. 22

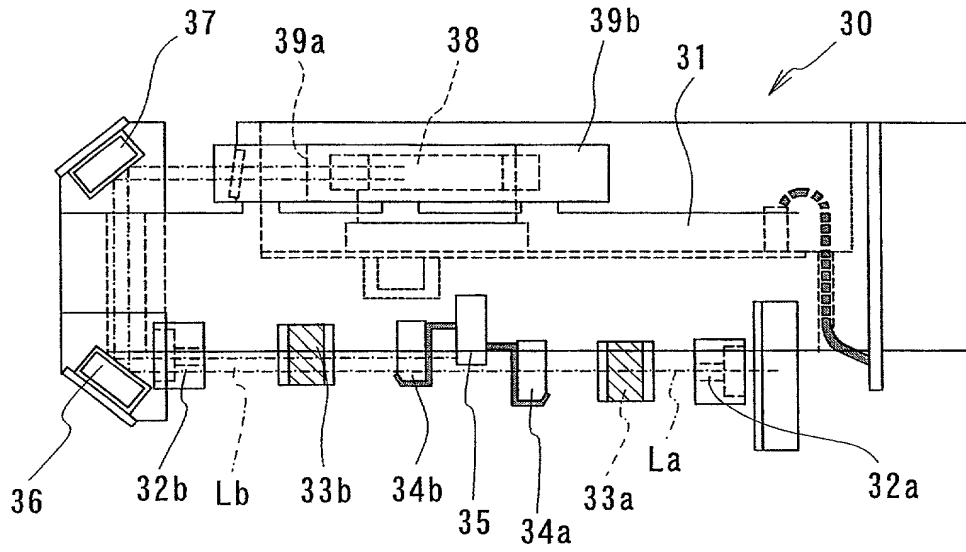


Fig. 23

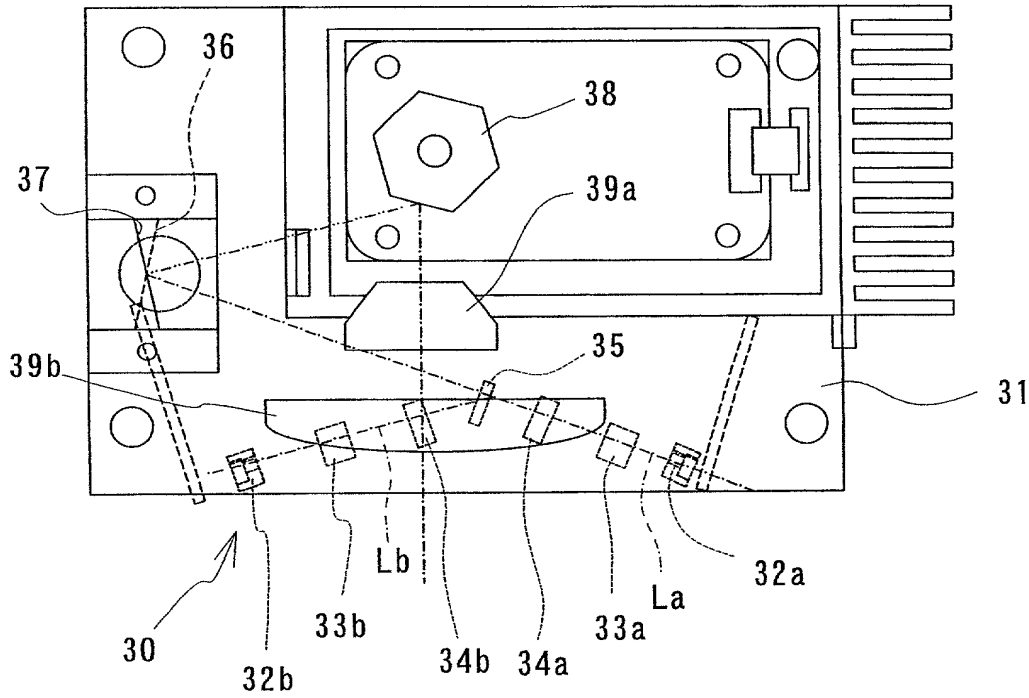


Fig. 24

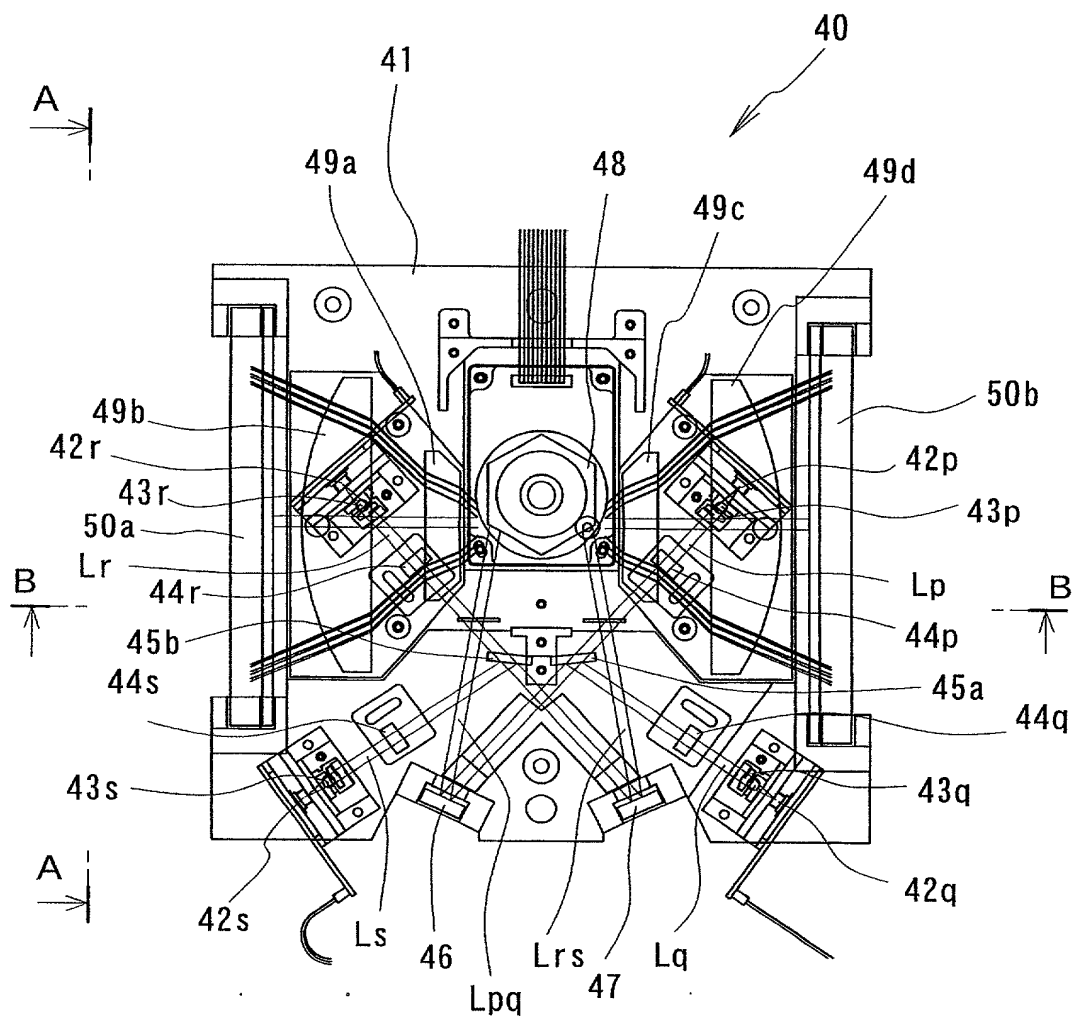


Fig. 25

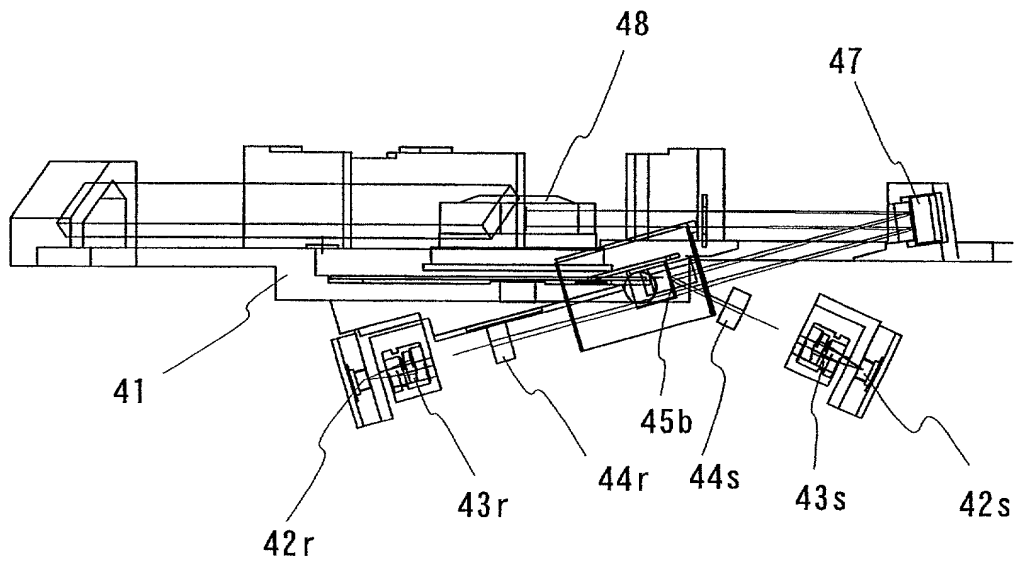


Fig. 26

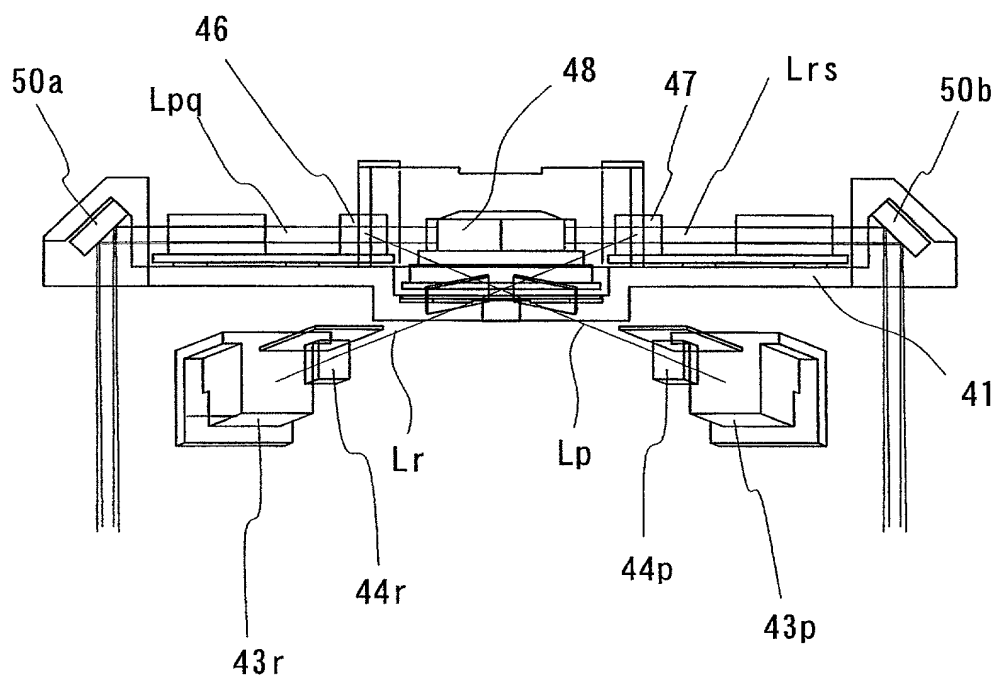
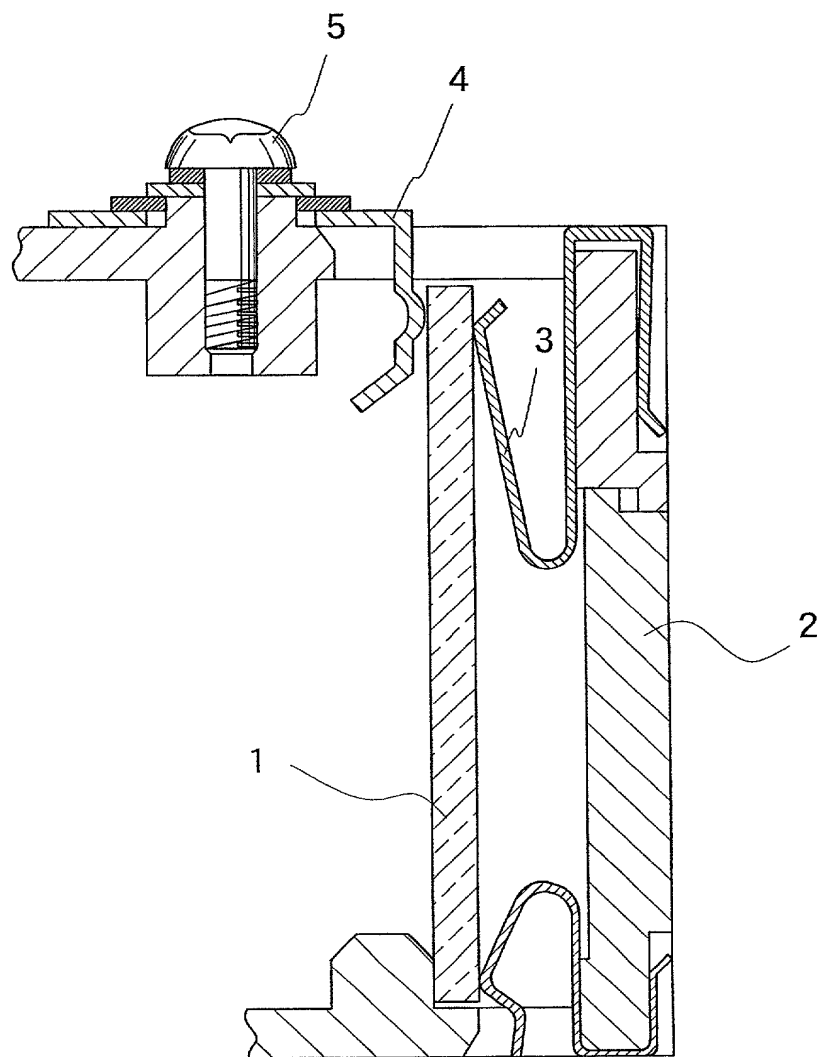


Fig. 27



(PRIOR ART)

Fig. 28